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Rapid Thermal Annealing of Oxide Electrodes for Nonvolatile Ferroelectric Memory Structures

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Abstract. We report on the properties of a ferroelectric stack comprising $(La_{0.5}Sr_{0.5})CoO_3$ (LSCO)/ $Pb(Nb,Zr,Ti)O_3$ (PNZT)/LSCO deposited on 4 inch diameter platinized Si wafers ($Pt/Ti/SiO_2/Si$). The LSCO electrodes were deposited at room temperature by pulsed laser ablation and the ferroelectric layer was deposited by the sol-gel technique. Rutherford backscattering was performed to confirm the uniformity in composition, thickness and stoichiometry of LSCO across the wafers. Conventional furnace or rapid thermal annealing was performed to crystallize the electrodes. The oxidation resistance of the conducting barrier layers, Pt/Ti, was found to be dependent on the annealing procedure adopted for the bottom electrode. In the case where the bottom LSCO was crystallized by rapid thermal annealing, Rutherford backscattering analysis and transmission electron microscopy studies revealed that there was no oxidation of the Pt/Ti conducting barrier composite. This is in contrast to the observations for in-situ deposition or conventional furnace annealing of the bottom electrode. The resistivity, coercive field and polarization of the ferroelectric stack were uniform across the 4-inch wafers. The ferroelectric capacitors showed no fatigue up to 10^{11} cycles and no imprint at 100°C. The ferroelectric properties were independent of the annealing procedure used for crystallizing the electrodes.

Keywords: ferroelectric, rapid thermal annealing, conducting barriers, oxidation resistance, resistance, oxide electronics

Introduction

The concept of using ferroelectric materials for memory applications has been investigated for several decades. However, materials problems and reliability issues have slowed their introduction into the market place. In the recent past there has been a significant upsurge in research efforts designed to address these materials issues, i.e. identification of an appropriate electrode technology and a suitable ferroelectric layer. For example oxide electrodes such as RuO_2 [1], IrO_2 [2–4], $SrRuO_3$ [5] and $La_{0.5}Sr_{0.5}CoO_3$ [6–7] have been found to improve the reliability of lead based ferroelectrics, such as $Pb(Zr,Ti)O_3$, $(Pb,La)(Zr,Ti)O_3$ and $Pb(Nb,Zr,Ti)O_3$. Similarly the layered perovskite, $SrBi_2Ta_2O_9$ when coupled with Pt electrodes has shown desirable ferroelectric properties [8–9]. Although materials solutions have been developed to address the reliability issues, there remains the outstanding issue of an appropriate conducting barrier layer(s) to integrate these capacitors into a commercially viable high-density memory technology. Figure 1 shows a schematic of such a vertically integrated high-density memory architecture. The barrier layers

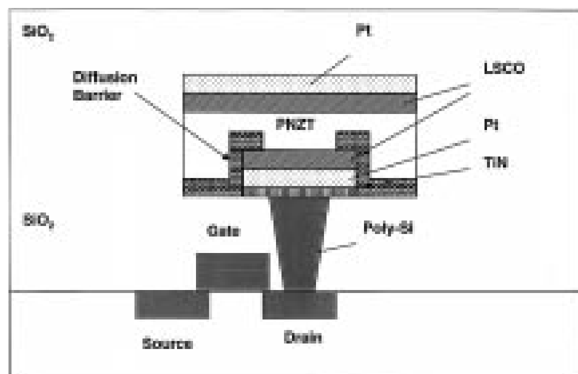

Fig. 1. Schematic diagram of a high-density memory architecture.

must prevent the diffusion of oxygen to the poly-Si plug and remain electrically conducting. Furthermore, they must neither react with Si nor allow the diffusion of Si to the ferroelectric capacitor or vice-versa.

TiN was the natural choice for such a barrier layer, since it was already being used in the semiconductor industry [10–11]. Unfortunately, TiN oxidizes at $\sim 500°C$ [12] whereas the optimum temperature is $\sim 600°C$ [13] for processing lead-based ferroelectric oxides and $\sim 800°C$ [8] for $SrBi_2Ta_2O_9$. Since Pt does not oxidize at these temperatures, Pt/TiN or Pt/Ti composites are being explored for use as barrier layers. Unfortunately, though Pt does not oxidize at these temperatures it cannot prevent oxygen from diffusing to the layers below it. Since oxygen diffuses through the grains and along the grain boundaries of Pt, controlling the thickness and crystalline quality of Pt would control the amount of oxygen that diffuses to the TiN surface. For example, epitaxial Pt/TiN barrier composites have been demonstrated to be oxidation resistant up to 650°C [14–15]. However, the high-density architecture of ferroelectric oxide hetero-structures grown on silicon would be polycrystalline. This necessitates the development of new approaches to improve the oxidation resistance of polycrystalline conducting barriers. One possibility is to lower the processing temperatures and to limit the exposure time to oxygen. During high temperature deposition of LSCO and PZT layers, the barrier composite (Pt/Ti) is exposed to gaseous oxygen and ionic oxygen diffusing through LSCO. To significantly reduce the exposure to gaseous oxygen these layers can be deposited at room temperature and then crystallized by conventional furnace annealing (CFA) or rapid thermal annealing (RTA). The structural integrity of the conducting barrier layers and the crystallinity of the layers deposited directly on the Pt surface would then be determined by the annealing conditions. In this study we have compared the effects of ex-situ annealing versus RTA on the structural integrity of Pt/Ti conducting barrier composite and the crystallinity of the LSCO electrodes.

Since there is a strong dependence of material properties on microstructure which in turn is determined by the processing technique employed, the choice of deposition technique for these materials is an equally important issue. Although, pulsed laser deposition (PLD) is not considered the deposition technique of choice for large area deposition it has several advantages compared to other physical vapor deposition techniques. For example, it is simple, flexible, allows for relatively high growth rate and stoichiometric transfer of target material. These advantages are very compelling in a research environment and therefore this technique has been widely used to deposit thin films of, for example, high $T_c$superconducting materials [16–17] and ferroelectric materials [18–20]. Transition of a laboratory scale PLD process to a manufacturing environment first requires that the films be deposited on large wafers. For example, Greer and Tabat [21] deposited Y-Ba-Cu-O superconducting thin films on 6-in wafers by PLD. However, there have been very few demonstrations of the uniformity of the PLD process over large wafers (i.e., > 4-inch diameter), especially in terms of the relevant physical properties. Bearing this in mind, in this study we have used the LSCO/PNZT/LSCO capacitor stack as a simple demonstration vehicle for scaling PLD to 4-inch wafers. We have also investigated the effect of annealing conditions used to crystallize the LSCO electrodes on the ferroelectric properties of the capacitors and the oxidation resistance of the conducting barrier layers.

Experimental Details

100 nm of $(La_{0.5}Sr_{0.5})CoO_3$ (LSCO) was deposited on 4 inch diameter platinized Si wafers, i.e. Pt(150 nm)/Ti(50 nm)/SiO_2(1000 nm)/Si wafers at room temperature by PLD using polycrystalline LSCO targets. Uniform large area films were obtained utilizing a rotating substrate and a large-diameter rotating target in conjunction with a rastered laser beam. The process was based on the approach discussed in some detail by

Greer [22]. To verify the uniformity in thickness, composition and stoichiometry of the LSCO layer, Rutherford backscattering was performed on samples randomly selected across a given wafer. The amorphous LSCO layer was crystallized by CFA in air for 1 h at 650°C. A ferroelectric layer, $Pb(Nb_{0.01}Zr_{0.445}Ti_{0.545})O_3$, (PNZT) of $\sim$200 nm was deposited by a sol-gel technique using lead (IV) acetate, titanium isopropoxide and zirconium-n-butoxide solutions. The Zr, Nb and Ti precursor solutions were taken in stoichiometric proportions and dissolved in hexane. This solution was spin coated on to the crystallized LSCO bottom electrode and dried at 300°C for 30 min to remove the organics. Additional film coatings were deposited after the above thermal treatment. The ferroelectric film was annealed at 650°C for 30 min. The top LSCO layer was deposited and crystallized in a fashion similar to the bottom LSCO layer.

The following procedure was used to check the uniformity in the electrical properties of the ferroelectric stack. A one-inch strip was cut from the 4-inch wafer along a diameter (Fig. 2), which was then sub-divided into five pieces. Electrical testing on all samples was performed by delineating capacitors with Pt dots of 50 μm diameter on the LSCO top electrode using a photolithographic lift-off process. The exposed top LSCO layer was then etched by nitric acid to isolate the individual capacitors. Contact to the bottom electrode was achieved by capacitive coupling through a large Pt contact on the wafer. The Pt electrode was a one inch strip $\sim$2 mm in thickness. All polarization-voltage (P-V) hysteresis loops were measured using a Radiant Technologies pulsed testing system (RT66A). Coercive voltage and pulsed polarization measurements were performed on capacitors in a row. Arbitrarily chosen capacitors were used for fatigue and imprint tests.

To investigate the effect of processing on the oxidation resistance of the Pt/Ti barrier layers, amorphous LSCO was crystallized by RTA at 700°C for 5 min. In this case, the top LSCO electrode was also crystallized by RTA. These samples were also prepared for transmission electron microscopy (TEM) studies to investigate the structural integrity of the Pt/Ti barrier composite.

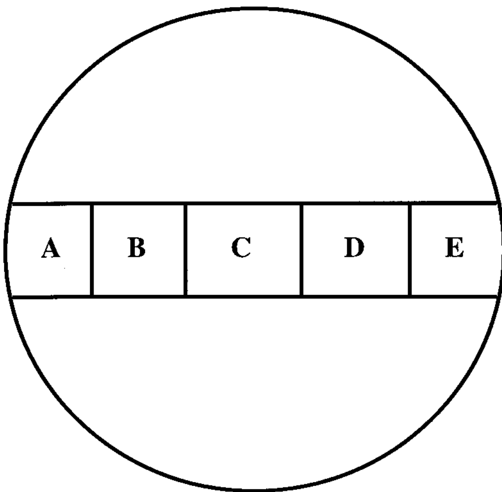

Fig. 2. Schematic diagram depicting the location from where the five samples were cut and processed to test the uniformity of the ferroelectric properties across a wafer

Results and Discussion

Figure 3 summarizes the results based on fitting RBS spectra that were collected for LSCO samples randomly selected across a given wafer. It is clear that both the thickness and the composition of the LSCO film are uniform across the wafer. Further, both reflect their nominal values, i.e. 100 nm, and $La/Sr = 0.5/0.5 = 1$ and $(La + Sr)/Co = 1$. The electrical resistivity for this composition is the lowest ($\sim$100 $\mu\Omega$cm) and therefore most desirable as an electrode. Any deviations from this composition, for example Sr content less than 0.5, would reduce the number of holes, thereby decreasing the

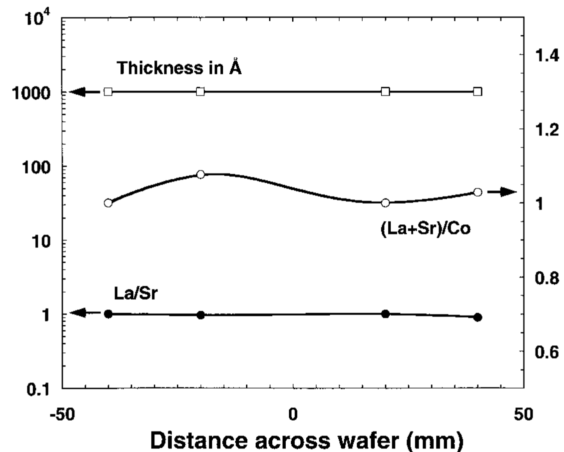

Fig. 3. Thickness and composition profile of LSCO across the 4-inch wafer.

conductivity of the film. The ferroelectric PNZT was deposited by sol-gel, which is an accepted technique to obtain uniform deposition. X-ray diffraction measurements confirmed perovskite phase purity of the LSCO and PNZT layers as well as the absence of pyrochlore or fluorite type phases. Figure 4 displays the X-ray diffraction spectra for two ferroelectric stacks. The bottom spectrum is for the ferroelectric stack where the LSCO electrodes were crystallized by CFA whereas the upper spectrum is for the stack where RTA was used for crystallization. The PNZT layers are polycrystalline with (001), (002) and (110) peaks as marked on the spectra. For LSCO, only the (110) peak is observed and its intensity and width is dependent on the type of annealing procedure adopted. In the case where RTA was performed to crystallize LSCO the (110) peak is broader indicating a smaller grain size. This was confirmed by an assessment of the grain size from deflection images obtained for the two samples using atomic force microscopy (AFM). The grain size of the LSCO crystallized by RTA was determined to be ~ 10 nm as compared to ~ 100 nm for the LSCO crystallized by CFA.

The capacitive coupling technique described earlier was used to measure the resistivity, coercive voltage (voltage required to switch the ferroelectric) and pulse polarization (difference between the switched and non-switched remanent polarization) of the ferroelectric capacitors. The uniformity tests were performed at 5 V. The resistivity was of the order of $\sim 10^9 \Omega$cm and the coercive voltage varied between 1.1 and 1.3 V. The mean value of the remanent polarization was $\sim 16\,\mu$C/cm^2, see Fig. 5. The spread in remanent polarization values across the wafer was between 12 and 20 μC/cm^2, which could be due to local variations in Pb content of the ferroelectric film. Nevertheless, the values are within two standard deviations of the mean value verifying the uniformity of the LSCO electrodes and the PNZT ferroelectric layer.

Polarization-field hysteresis loops for typical capacitors from samples with LSCO crystallized by CFA and from samples with LSCO crystallized by RTA are plotted in Fig. 6. Note that the capacitors are symmetric along the voltage axis in both cases and that the coercive field and remanent polarization values, i.e. $2P_r$ values are similar. This suggests that these properties of the ferroelectric layer are not dependent on the grain size of the oxide electrodes. Figure 7 is a plot of the pulse polarization and coercive field as a function of applied field for the two different types of samples investigated in this study. It is clear that the trends for both samples are nearly identical, which also indicates that the electrical properties do not depend on the grain size of the LSCO electrodes. Both capacitors saturate at 250 kV/cm with coercive fields of ~ 55 kV/cm and remanent polarization values of $\sim 22\,\mu$C/cm^2.

When ferroelectric memory devices are integrated with current semiconductor technology, they are likely to undergo a large number of read/write cycles to retrieve/store information making it vital

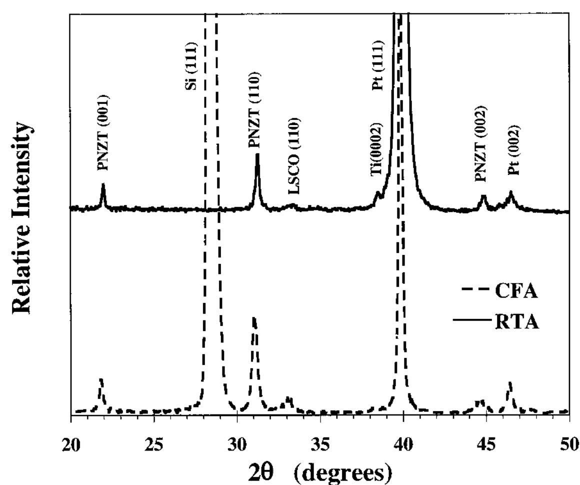

Fig. 4. X-ray diffraction spectra for the ferroelectric stack, LSCO/PNZT/LSCO, on Pt/Ti/SiO_2/Si where the LSCO was crystallized either by RTA or CFA.

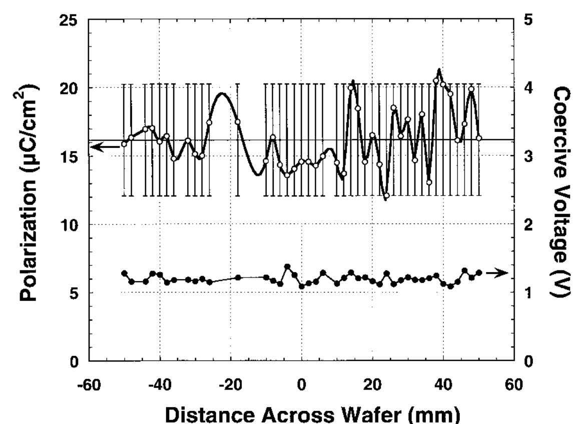

Fig. 5. Remanent polarization and coercive voltage of the ferroelectric capacitors across the 4-inch wafer measured at 5 V.

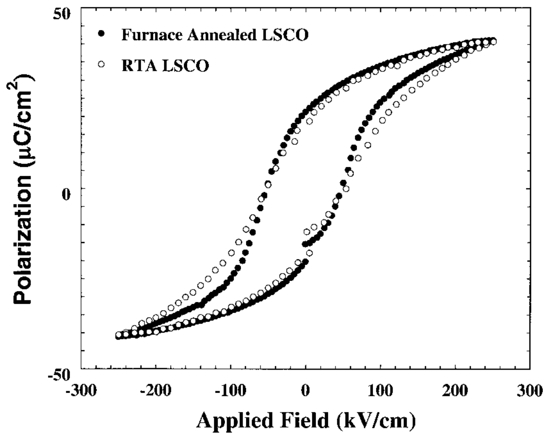

Fig. 6. Hysteresis loop measured at 250 kV/cm for typical capacitors from a sample with the electrodes crystallized by CFA and a sample with LSCO crystallized by RTA.

that they have long-term reliability. Repeated read/write cycles are simulated with polarization reversals. Any loss in switchable polarization is then a measure of fatigue. Several studies have shown that lead based ferroelectric capacitors with LSCO electrodes exhibit almost no fatigue up to 10^{11} reversals [23–25]. The excellent performance of the capacitors is credited to the LSCO electrodes, which unlike metal electrodes can act as efficient sources and sinks for oxygen vacancies. In this study we compared the fatigue performance for samples with both CFA and RTA crystallized LSCO electrodes. In the fatigue test, 1 MHz bipolar square pulses of effective field strengths of 250 kV/cm were applied as fatigue stress on the capacitors. Figure 8(a) and 8(b) plot the results from such bipolar fatigue tests conducted at room temperature for typical capacitors on the two samples. The remanent polarization values are plotted as a function of fatigue cycles and in both cases the capacitors exhibit almost no fatigue up to 10^{11} cycles. To further evaluate the quality of the capacitors, fatigue tests were also performed at lower frequencies, viz. 1 kHz and 10 kHz, with similar stress fields. In these cases also the capacitors exhibit no polarization loss at least up to 10^8 cycles.

Another reliability concern for ferroelectric memory devices is imprint, which is defined as the preference of a ferroelectric capacitor for one state over the other [26]. This preference manifests itself as

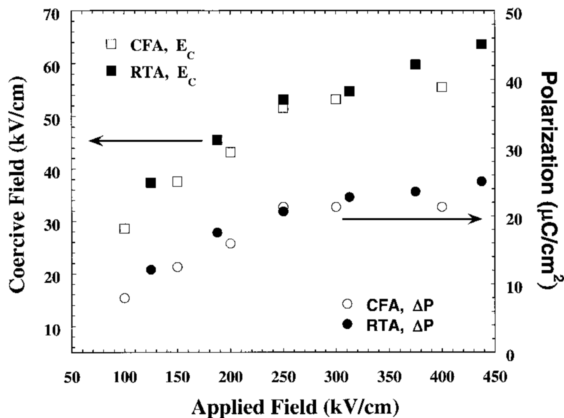

Fig. 7. Remanent polarization and coercive field as a function of applied field for capacitors with the LSCO crystallized either by RTA or CFA.

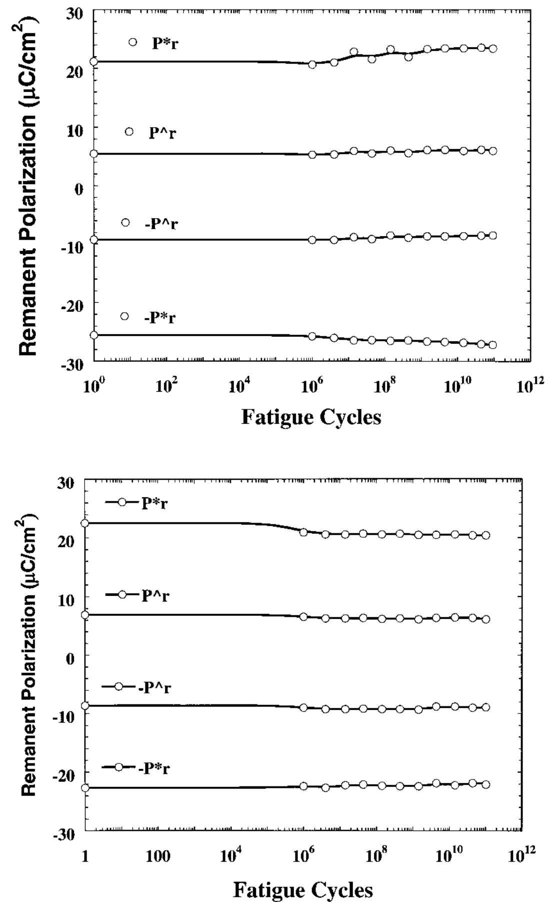

Fig. 8. Remanent polarization values as a function of fatigue cycles at room temperature for an arbitrarily chosen capacitor on a sample where (a) LSCO was crystallized by CFA and (b) LSCO was crystallized by RTA. The fatigue test was performed using square pulses of effective field 250 kV/cm at 1MHz.

an asymmetry along the voltage axis in the hysteresis loop of the capacitor. As a result, one state has a lower coercive field as compared to its complementary state. The asymmetry is a result of an internal field, which could develop due to repeated access of one state. An accelerated test to investigate the tendency of capacitors to imprint is to subject them to unipolar pulses at an elevated temperature. Our imprint test protocol involved subjecting a capacitor to 10^8 single sided pulses of 5 V at 100°C. Figure 9(a) is a plot of the hysteresis loops before and after imprint test for a capacitor where the LSCO was crystallized by CFA. Figure 9(b) is a similar plot for a capacitor where the LSCO was crystallized by RTA. Despite our rigorous test protocol, neither capacitor shows any sign of imprint indicating robust capacitors.

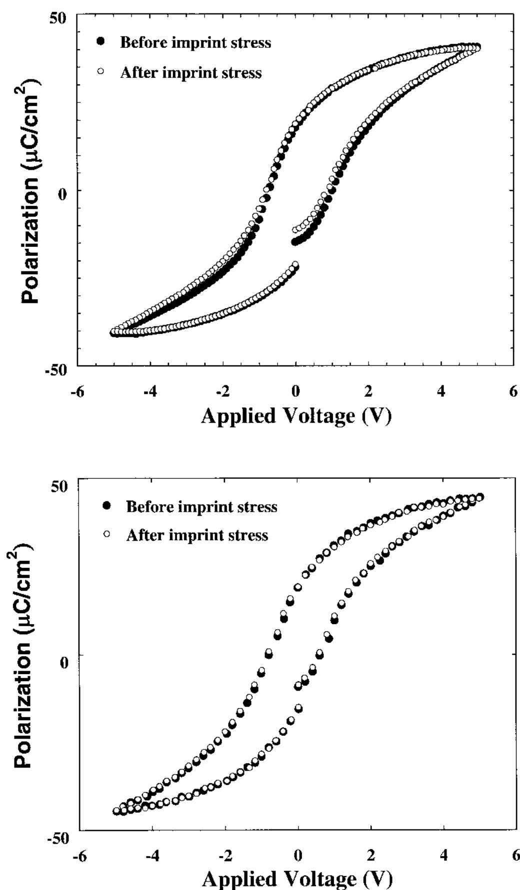

Fig. 9. Polarization-voltage hysteresis loops before and after 10^8 +5 V pulses at 100°C for an arbitrarily chosen capacitor on a sample where (a) LSCO was crystallized by CFA and (b) LSCO was crystallized by RTA.

Once the reliability of the ferroelectric capacitors was verified the structural integrity of the Pt/Ti conducting barrier stack was investigated. The integrity of the conducting barrier composite will depend both on the processing temperature and the time that it is subjected to at those temperatures. The bottom LSCO electrode can either be deposited in-situ at ~650°C in an optimized oxygen ambient, or deposited at room temperature and then crystallized later either by CFA or RTA. Earlier studies show that when Pb-Zr-Ti-O is deposited in-situ, the Ti layer oxidizes to form TiO_2, which exhibits a granular structure and leads to hillock formations on the Pt surface [27]. Furthermore, there is interdiffusion between the Ti and Pt layers; Ti diffuses through Pt to the surface and oxidizes to form TiO_2 and Pt in turn diffuses into the Ti layer. One can expect a similar situation for the case when LSCO is deposited in-situ. This is the main impetus for a room temperature deposition of LSCO with an ex-situ crystallization process.

Figure 10 is the RBS corresponding to the Ti peak obtained from a LSCO/Pt/Ti/SiO_2/Si sample, where the LSCO is amorphous and the substrate has not been subjected to high temperature. At this stage there is no oxidation of Ti or any reaction between Ti and its adjacent layers. Also plotted in Fig. 10 are the spectra for a sample with CFA (650°C, 1 h) crystallized LSCO and a sample with RTA (700°C, 5 min.) crystallized LSCO. The spectra for the Ti peak in the case of CFA

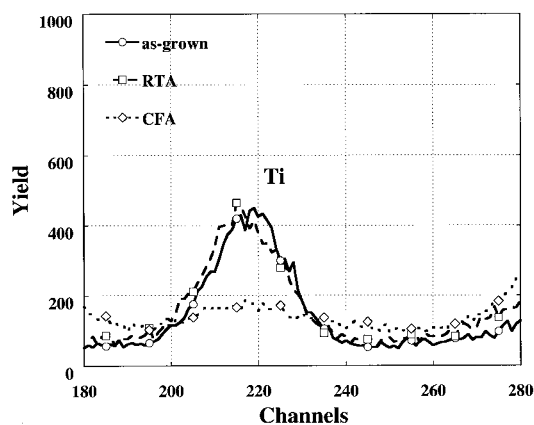

Fig. 10. Rutherford backscattering spectra for LSCO/Pt/Ti/SiO_2/Si corresponding to the Ti peak for an as-deposited LSCO sample, a sample where LSCO was crystallized by CFA and a sample where LSCO was crystallized by RTA.

shows significant broadening and a lowering of intensity, which is suggestive of oxidation of Ti and possible diffusion into adjacent layers. A fitting of the entire spectrum indicates that there is interdiffusion between Ti and Pt and TiO_2 is formed. Thus, CFA of the amorphous LSCO layer also leads to similar problems as those during in-situ deposition of LSCO. In contrast, there is no change in the Ti peak spectrum for the case where LSCO was crystallized by RTA, indicating that the Ti layer maintains its structural integrity. TEM studies were performed to confirm this observation.

Figure 11 is a cross-sectional bright-field TEM image of the Pt/Ti interface from a LSCO/PNZT/LSCO/Pt/Ti/SiO_2/Si sample, where the LSCO is crystallized by RTA. Notice that the Ti/Pt interface does not show any reaction. More importantly Ti is not oxidized as evidenced by the absence of hillocks and bright regions in the Ti layer. The expected columnar structure of Pt is seen clearly with no reaction phases along its grain boundaries. This image is a direct verification of both the absence of interdiffusion between the two layers and the lack of any oxide formation during annealing. The inset of Fig. 11 shows the X-ray diffraction pattern for the ferroelectric stacks with RTA and CFA crystallized LSCO electrodes. Note that only the samples with LSCO crystallized by RTA showed a peak at 38.41°,

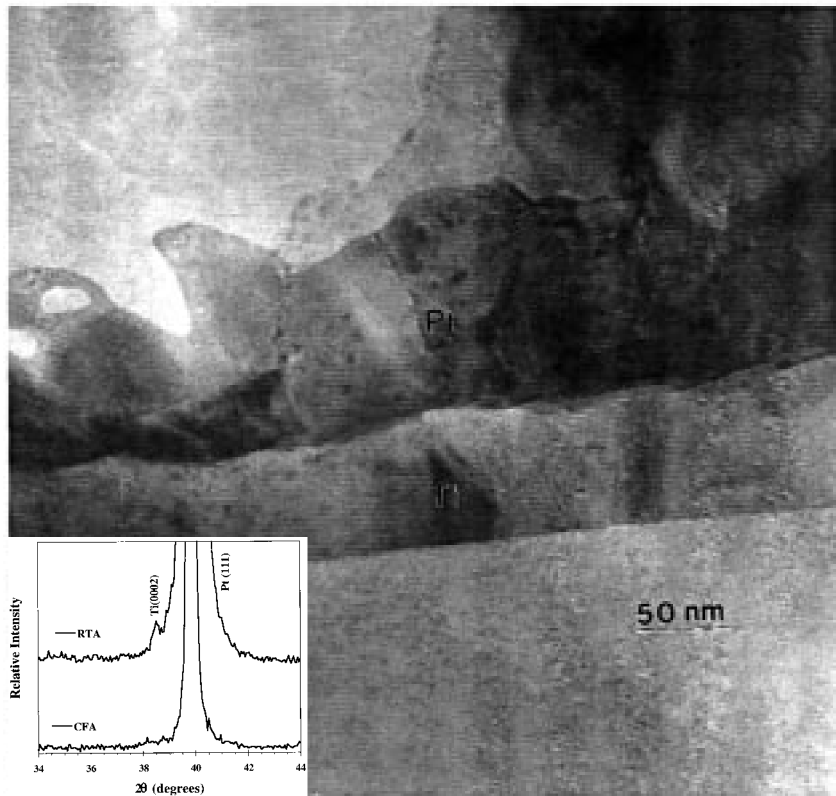

Fig. 11. Cross-sectional bright-field TEM image of a LSCO/PNZT/LSCO/Pt/Ti/SiO_2/Si sample, where LSCO was crystallized by RTA showing the Pt/Ti interface indicating no interdiffusion between Pt and Ti and no oxidation of Ti. Inset is the X-ray diffraction pattern clearly showing the Ti (0002) peak.

which corresponds to (0002) Ti. One may argue that this peak can be assigned to PNZT (111). We believe that this peak is not from PNZT, since it is not present in both the spectra although the processing of the ferroelectric layer in both the samples was similar. These diffraction patterns conclusively demonstrate that Ti does not oxidize or react with Pt when RTA crystallizes the LSCO electrodes. Figure 12 is a cross-sectional bright-field TEM image of the Pt/Ti interface, where the LSCO is crystallized by CFA. Notice that the Ti layer is oxidized as evidenced by the granular microstructure of TiO_2. Furthermore, these granular formations are clearly visible in the grain boundaries of the columnar Pt layer also.

Based on our results, we can now make the following comments concerning the differences between the three techniques, viz. in-situ deposition, CFA and RTA. During in-situ deposition, there is gaseous oxygen available at the interface so oxygen can diffuse along the grain boundaries of Pt to oxidize Ti. Furthermore, the temperature and time of deposition allows for interdiffusion to occur between Pt and Ti. Ex-situ CFA in oxygen ambient seems to produce similar results. In this case, however the oxygen must diffuse through the LSCO to the Pt/Ti interface. During RTA, the two layers are exposed to the annealing temperature for a much shorter time. Also, there is no free oxygen at the Pt surface. It should be mentioned that RTA has been widely used to crystallize the Pb-Zr-Ti-O layer and some studies report similar results [28–29]. In these studies, the interface between Pt and the ferroelectric also showed no evidence of reaction.

Conclusions

$La_{0.5}Sr_{0.5}CoO_3$ was deposited by PLD on 4-inch diameter platinized silicon wafers. RBS data shows that these films are stoichiomteric, homogeneous in composition and uniform in thickness (~ 100 nm) across the wafer. The resistivity, coercive voltage and remanent polarization of the ferroelectric stack, LSCO/PNZT/LSCO, were measured across the wafer and found to be uniform. RTA or CFA was performed to crystallize the LSCO electrodes and the grain size was ~ 10 nm and ~ 100 nm respectively. However, the ferroelectric properties of the capacitors were independent of the grain size of the LSCO electrodes. The capacitors exhibited coercive fields of ~ 55 kV/cm and polarization values of $\sim 22\,\mu C/cm^2$ at 250 kV/cm. The capacitors showed no fatigue up to 10^{11} cycles and no imprint at 100°C. When the LSCO electrodes were crystallized by CFA, the structural integrity of the Pt/Ti layer was compromised. However as verified by X-ray diffraction, cross-sectional TEM images and RBS spectra, when the LSCO electrodes were crystallized by RTA there is no

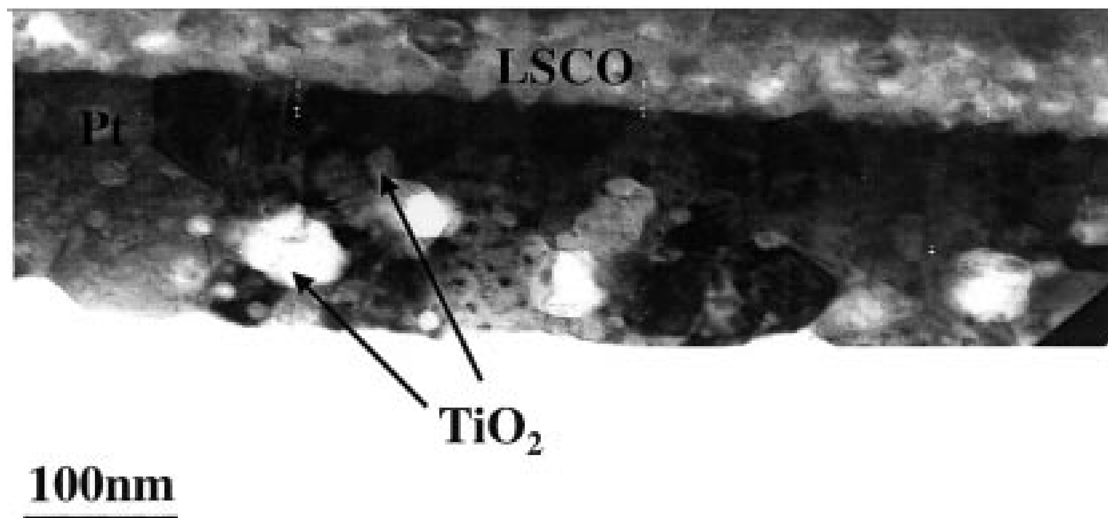

Fig. 12. Cross-sectional bright-field TEM image of a LSCO/PNZT/LSCO/Pt/Ti/SiO_2/Si sample, where LSCO was crystallized by CFA showing that the Ti layer is oxidized and TiO_2 is formed in the grain boundaries of Pt.

interdiffusion between Pt and Ti and no oxidation of Ti. It is imperative to continue to identify viable conducting barrier layers to fabricate high-density memories. Several research institutions and industrial laboratories have intensive ongoing efforts in this direction. The results from this study demonstrate that RTA may provide a solution to the very challenging problem of conducting barrier layer oxidation during growth of ferroelectric capacitors in the high-density memory architecture.

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